Electronic packaging structure with integrated distributed decoupling capacitors

The invention relates to an electronic packaging structure, comprising a substrate, a first electrode layer on a first side of said substrate, dielectric material arranged in a preselected pattern on said first electrode layer and a second electrode layer forming a plurality of second electrode layers arranged on said preselected pattern of dielectric material to form a distributed capacitive structure together with said first electrode layer as a first decoupling stage. The invention further relates to an integrated circuit incorporating the electronic packaging structure of the invention.

Powering of systems on chip that incorporate high-speed digital cores operated by high current and low voltage requires both high speed power modules and lowest parasitic passives within in the power delivering network to avoid noise to the greatest possible extent.

It is well known technique for reducing the level of noise to arrange discrete capacitors between associated voltage pins. The discrete capacitors, normally mounted a distance away from the semiconductor core, are electrically coupled thereto by a plurality of power wiring lines or large power busses. These power wiring lines typically represent high inductant paths which should be minimised by moving the discrete capacitors as close to the semiconductor chip as possible. Regarding the high frequency decoupling capacitance mounted closest to the core, its characteristics in terms of parasitic impedance determines the maximum current transients and thus the systems speed. The more ideally this capacitance behaves, the more the current transients can be shifted to higher values at given tolerances for the allowed voltage fluctuation and high frequency oscillations.

US 4,945,399 discloses an electronic packaging structure which includes a plurality of integrated, distributed decoupling capacitors. A bottom layer of metal, formed on a substrate, includes at least one portion which forms a first plate of a

decoupling capacitor and includes at least one electronic connection for attachment of a semiconductor chip. A thin layer of dielectric material covers the bottom layer. A top layer as the second plate of the capacitor is formed on the dielectric material and is positioned relative to the first plate to form the decoupling capacitor. This structure can be arranged beneath the die of a chip. The length of connectors is kept to a minimum in order to minimise any inductance created thereby and to bring the decoupling capacitor as close as possible to the die.

It is an object of the present invention to provide a further improved electronic packaging structure.

This object is achieved in an electronic packaging structure as defined above by a second decoupling capacitor stage of high capacitance which is arranged on a second side of said substrate opposite said first side and it is electrically connected to said distributed capacitive structure. The capacitance of that second decoupling capacitor stage is high enough to provide a low impedance connection to the power sink, and may be higher by a factor 5 to 100, preferably about 10, than that of the first decoupling stage.

It should be noted that the pattern of dielectric material and second electrodes depends on the pitch of the connectors to the chip to be supplied with power.

Said distributed capacitive structure which has an extremely low series inductance and dielectric material of extremely high permittivity of 1000 or more can be mounted directly under the die or its substrate and carries on the side opposite thereto the elements providing the next filter stage. Therefore, not only the distributed electrode structure can be coupled in an optimum low inductive way to a power sink but also the second decoupling capacitor stage yielding a considerable improvement of decoupling in the high frequency range.

In a preferred embodiment, said distributed capacitive structure consists of alternating polarities in a first direction on said substrate and of alternating polarities in a second direction on said substrate which is substantially perpendicular to said first direction. Thereby, a fine-meshed capacitance area consisting of a common electrode mounted between a substrate and a dielectric material is provided. The distributed

capacitance structure consists of a high number, e.g. 100, of individual cells in parallel.

To realise this effectively, contact areas to said first electrode layer can be formed in apertures of said preselected pattern of said dielectric material to provide one of said polarities of said distributed capacitive structure. Since the alternating polarities are arranged closely adjacent to another, high frequency peaks are filtered out, because this arrangement exhibits minimum inductance.

Preferentially, said substrate comprises throughholes provided for connecting said distributed capacitive structure and said second decoupling capacitor stage. The skilled person will appreciate that said throughholes extend equally through said first electrode layer and are part of the preselected pattern of said dielectric material, if necessary.

Also said second decoupling capacitor stage may consist of a plurality of capacitors.

Said substrate can be made of conductive material, for example of conductive silicon (Si).

An integrated circuit can be built, comprising a processor and an electronic packaging structure of the invention, wherein preferably said second electrode layer of the electronic packaging structure face said processor.

The electronic packaging structure of the invention provides a module having a reduced parasitic impedance in terms of inductance and resistance. Supply voltage fluctuations due to the resistive and inductive voltage drop are reduced which allows apply higher current transients. Consequently, the excitation of supply line oscillation occurs only at higher frequencies and reduced amplitude. Signal integrity problems caused by EMI will be substantially alleviated.

A typical application of the invention is in a power delivery network as a connection between a power supply unit, e.g. a voltage regulator module (VRM) and a load. Regularly, such power delivery network comprises a number of power filter stages, for socket and also a decoupling capacitance as integral component of the chip itself. Two trends are observed when going the route from the voltage regulator module to the chip. The capacitances of the capacities become smaller, as well as the impedances of the connecting inductivities and resistances and also the parasitic series inductivities and resistances of the capacitors. This means that the energy which can be

stored in the capacitors in decreasing distance to the load becomes smaller, the energy, however, because of the very small impedances in the immediate neighbourhood is rapidly available. High frequent load steps are filtered by the components in its near region, low frequent load steps, which are representing longer lasting changings of the current needs, are covered mainly by large capacities in the further surroundings, whereas the voltage regulator module itself must be capable to follow far slower changes in the load. Therefore, the power delivery networks includes an arrangement consisting of filter stages which are finely tuned among another and also to the load, the characteristics thereof being permanently optimized with respect to parasitic impedances. In the invention, the first filter stage provides a plurality of capacities or even a distributed capacitance which is connected to the chip in a considerable low inductive manner and comprising a comparatively low capacitance, this means comparatively low storable energy which is rapidly available. Further, the module already comprises the second filter stage (i.e. the second decoupling capacitor stage) adjacent thereto, having by a factor of about 5 to 100 larger energy storages in form of discrete capacitors, e.g. multi layer ceramic capacitors. Compared to structures known hitherto, these capacitors of said second filter stage are connected to the first filter stage at a comparatively low impedance, however, due to the through contacting, it is a rather high impedant connection to the first filter stage.

The invention will be described in greater detail by referring to the accompanying drawings and the description that follows.

Fig. 1 shows in a vertical cross section the configuration of an electronic packaging structure according to the invention; and

Fig. 2shows a top view on a part of the configuration of Figure 1.

In Figure 1, a dielectric material 1 is arranged between a first electrode 2 and a plurality of second electrodes 3. The dielectric material is, for example, a thin ceramic having a relative permittivity of 1000 or more. Typical values of thickness of the dielectric material are 50 nm to 500 nm. The dielectric material 1 is structured to

provide access to the first electrode layer 2, so that contact areas 6 can be formed. Thus, a connector field of alternating polarities 5a and 5b is achieved. Flip-chip-solder bumps, for example, provide contact to each of the second electrodes 3 and the common first electrode layer 2 through the contact areas 6. The arrangement is carried on a substrate 4, which can be conductive in order to decrease the resistance and inductance of the first electrode 2 and to save through connections to electrodes 10. A plurality of discrete capacitors 9 is arranged beneath the substrate 4 to provide the second decoupling capacitor stage. An alternating polarity is given by electrodes 10 on the underside of said substrate 4 and conductive through platings 8 at the inside walls of throughholes 11 which are provided in substrate 4, first electrode layer 2 and dielectric material 1. An insulating lining 7 is brought into each throughhole to avoid contact of the plating with the first electrode layer 2 and conductive substrate 4.

Figure 2 shows a top view on the configuration of Figure 1. A mesh-like area of alternating polarities 5a, 5b is formed extending in two directions which are perpendicular with respect to another. The size of the individual capacitor cells is defined by a pitch 12 which in turn depends on the pitch (distance between connectors of the chip to be supplied with power).

A similar chequered pattern, however, showing a significantly larger pitch, is formed by the electrode connections for contacting said discrete capacitors 9 (second decoupling filter stage) at the bottom side of substrate 4.